Our Ref.: RamBus D-1

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office and citizenship are as stated below, next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled INTEGRATED CIRCUIT I/O USING A HIGH PERFORMANCE BUS INTERFACE the specification of which

__XX__ is attached hereto.

_____ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I do not know and do not believe that the same was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of

Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status-patented pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status-patented pending, abandoned)

I hereby appoint Roger S. Borovoy, Reg. No. 20,193, and David J. Larwood, Reg. No. 33,191, 600 Hansen Way, Suite 100, Palo Alto, California 94306, telephone (415) 856-9411, my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith. Please address all correspondence to Mr. Larwood.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventors: Michael Farmwald

Residence 82 Eucalyptus Rd., Berkeley, California 94705 (City, State)

Citizenship U.S.A. (Country)

Inventor's Signature Paul Michael Farmwald Date April 17, 1990

Full Name of Joint/Second Inventor: Mark Horowitz

Residence 2024 Columbia Street Palo Alto, California 94306

Citizenship U.S.A. (Country)

Inventor's Signature Mark Horowitz Date April 17, 1990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. **RA043D2DC**)

In the Application of:	)	
	)	
FARMWALD ET AL.	)	**Group**
	)	**Art Unit:**
Serial No: CONTINUATION OF 09/161,090	)	
	)	**Before**
Filed: Herewith	)	**Examiner:**
	)	
Title: INTEGRATED CIRCUIT HAVING MEMORY WHICH SYNCHRONOUSLY SAMPLES INFORMATION WITH RESPECT TO EXTERNAL CLOCK SIGNALS	)	

Assistant Commissioner for Patents
Washington, DC 20231

POWER OF ATTORNEY BY ASSIGNEE,
REVOCATION OF ALL PRIOR POWERS OF ATTORNEY
AND
CERTIFICATE UNDER 37 CFR 3.73(b)

Sir:

The undersigned, being empowered to sign this Power of Attorney, Revocation of All Previous Powers of Attorney and Certificate under 37 CFR 3.73(b) on behalf of Rambus, Inc., the assignee of the entire right, title and interest in the above-referenced application, hereby revokes all prior powers of attorney and hereby appoints Neil A. Steinberg, Reg. No. 34,735, with full power of substitution and revocation to prosecute this application and to transact all business before the United States Patent and Trademark Office in the above-referenced application.

Rambus, Inc., formerly a California corporation with a place of business at 4920A El Camino Real, Los Altos, California 94022, certifies that it is the assignee of the entire right, title and interest in the above-referenced patent application by virtue of an assignment from the inventors, Michael Farmwald and Mark Horowitz. The assignment of the parent patent application (Application Serial No. 07/510,898) and all continuing and divisional application thereof to Rambus Inc. was filed on April 18, 1990 and recorded in the U.S. Patent and Trademark Office at Reel 5385, Frame 875.

The undersigned has reviewed all the documents in the chain of title of the above-referenced application and, to the best of the undersigned's knowledge and belief, title is in Rambus, Inc., the assignee identified above.

Please direct all correspondence in the above-referenced patent application to:

Neil A. Steinberg, Esq.
Rambus Inc.
2465 Latham Street
Mountain View, California 94040
Telephone: 650-944-7772
Facsimile: 650-944-8080

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so

make are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon.

Date: April 10, 2000

Neil A. Steinberg, Esq.
Vice President
Intellectual Property
Rambus Inc.

-TRANSLATION-

PTO's Mailing Number: 223798
PTO's Mailing Date: August 8, 2000

NOTICE OF THE REASON FOR REFUSAL

Patent Application Number	:	508050/'91
Date considered by the Examiner	:	July 28, 2000
Patent Office Examiner	:	Minoru Taga
Attorney for the applicant	:	Masaki YAMAKAWA (and other five persons)

Being rejected under Patent Law Art. 29, Para. 2 and Art. 36 and Art. 37

The application identified above is refused for the reason noted below. Any argument in opposition should be filed within three months from the mailing date of this Notice.

REASON 1

The invention described in claims of this application can not be granted a patent because, in accordance with Article 29, Paragraph 2, it had been possible for a person of ordinary knowledge in the technological field to which the invention belongs to have invented such an invention with ease on the basis of the invention made known in Japan or in the foreign country in the publications below prior to the present application.

REMARKS

Regarding Claims 1 and 2: References 1 and 2 are cited.

Reference 1 describes a memory apparatus including a RAM coupled to a CPU via bus lines, wherein the CPU sequentially sends to the RAM via the bus lines a device ID, an operation code, a RAM address (one address is divided into three for separate transmissions) and data so as to make a request and the RAM in turn decodes them in order to send a response back to the CPU via the bus lines whereby any increase with the number of bus lines is prevented. Thus, the invention recited through present Claims 1 and 2 is not particularly different form the one described in Reference 1.

Reference 2, then, describes a semiconductor memory apparatus wherein operation mode information, an address and data are transmitted in a time-shared manner via address lines and the invention recited through present Claims 1 and 2 is not particularly different from the one described in Reference 2, either.

Regarding Claim 3: Reference 3 is cited.

The "control circuit 1", "modules 21~24" and "address set control signal lines 5 and 6" respectively correspond to the "master", "first memory", "second memory" and "reset signal" of the present invention.

Refer also to item (3) under Reason 2.

Regarding Claim 15: References 1 and 4 are cited.

[The first paragraph with respect to Claims 1 and 2 above is repeated here as what is described in Reference 1.]

The invention in Reference 1 is without a circuitry means equivalent to the circuit in item (D) of present Claim 15 but Reference 4 describes a data processing system having a CPU coupled to an n number of memory devices via a common bidirectional bus, wherein, according to a certain command from the CPU, the transmission-reception timing setting circuit of each of the said n number of memory devices is provided, for timings to be set, with transmission-reception timing information corresponding to the time periods required for wait until the data read out is permitted to be fed onto the said common bus, so that efficient data access to the memory devices can be possible by accessing the plural memory devices at those set timings, although a common bidirectional bus of narrow data width is used.

References 1 and 4 respectively relate to a system in which a CPU and a memory or memories are coupled via a common bidirectional bus to improve the process efficiency of the system while restraining the expansion of the data width of the bus. It is, therefore, readily conceivable by any person of ordinary skill in the art to achieve the present invention by applying the invention of Reference 4 to that of Reference 1 with the aim of further enhancing efficiency.

Regarding Claim 16: References 1 and 4 are cited.

To add to the explanation above with regard to Claim 15, the device ID is compared for verification before the memory concerned is activated in the invention of Reference 1, too, and no separate device-select lines are used.

Regarding Claim 17: References 1 and 5 are cited.

According to the invention in Reference 1, the first word in the packet is only a device ID, but an arrangement for transmitting in the first word a chip selection signal and part of an address is described in Reference 5.

Regarding Claim 18: References 1 and 5 are cited.

To add to the explanation above with regard to Claim 17, if the OP signal in the invention of Reference 1 is considered as a part of the bits of the packet, the OP signal can be regarded as information indicative of the start of the packet in the invention of Reference 1 as well.

Whether to send the information for controlling the operation of the memory (the operation code in Reference 1) before or after the device ID is construed as only a matter of planning readily available for choice by those skilled in the art when designing the format of the packet for a demand to the memory.

REASON 2

This application does not fulfil the requirements of Article 36, Paragraphs 5 and 6 with respect to the note(s) below concerning the descriptions in the specification and the drawings.

REMARKS

(1) There are used expressions "substantially less" and "substantially all" in Claims 1 and 2 but the word "substantially" makes unclear the standards of judgement of "less" and "all". Thus, the matters indispensable for the arrangements in the inventions applied to be patented are made ambiguous.

(2) [A typographical error is pointed out, which will duly be corrected.]

(3) Regarding the recitation of Claim 3

(a) The description reading "to reset identifiers of the first and second memories in response to the reset signal" can be understood to mean either

(i) that (the value of the register for storing the identifiers of the memories) is cleared as explained in lines [6-10 and 15-20 on page 37 of the original English specification] or

(ii) that identifiers are set in the register for storing the identifiers of the memories as explained in lines [10-14 on page 37 and line 21 on page 37 to line 14 on page 38 of the original English specification]

and is, therefore, ambiguous.

(b) According to the claim recitation, identification values are sent via a daisy-chained line but ID numbers are sent via BusData [0:3] according to the explanation in the specification [on page 37 of the original English specification]. Thus, the claim recitation and the detailed explanation of the invention are not in harmony.

There is described in lines [20-23 on page 38 of the original English specification] that "For instance, a series of sequential numbers could be clocked along the ResetIn line and at a certain time each device could be instructed to latch the current reset shift register value into the device ID register", which appears to mean such an address setting method as disclosed under the caption "Prior Art" and in Fig. 3 in microfilmed Utility Model Application No. Sho 60-42584 (Utility Model Application Laid-Open No. Sho 61-160556), for example, in which case address setting in the register circuit is carried out simultaneously in a plurality of devices to be controlled. Thence, this description does not match, either, the claim recitation suggesting that identification values are stored at "a first predetermined time" and "a second predetermined time" separately.

Thus, the invention recited in Claim 3 can not be said what is described in the detailed explanation of the invention.

(4) Regarding Claim 15

(a) There is mentioned that "the multiline bus has a total number of lines less than a total number of bits in any single address". It is not clear, however, as to whether it means

(i) that the total number of lines is less than the number of bits required for specifying an address in the space of the memory (specifically 16 if the memory space is 64K bytes), or

(ii) that the total number of lines is less than the bit width of the data that can be stored in an address.

(b) [A typographical error is pointed out, which will duly be corrected.]

(5) Regarding Claim 17

(a) The same as in item (4)(a) above.

(b) [A typographical error is pointed out.]

REASON 3

This application does not fulfil the requirements of Article 36, Paragraph 4 with respect to the note(s) below concerning the descriptions in the specification and the drawings.

REMARKS

There are some terms and expressions which can not be understood. The following are examples.

(i) [Simply a typographical error with] "the selected row" [in line 20 on page 24 of the original English specification]

(ii) [Regarding] "ResetIn combined with changeable values on the external bus" [in lines 12-13 on page 37 of the original English specification]

(iii) [Regarding] "to sink 50mA" [in line 2 on page 45 of the original English specification]

(iv) [Regarding] "precharged" [in line 7 on page 24 of the original English specification]

REASON 4

This application does not fulfil the requirements of Article 37 with respect to the note(s) below.

REMARKS

Unity of the inventions in Claims 1, 2 and 15-18 can be recognized with respect to the substantial parts of the indispensable claim elements that a request to the memory is made through signal lines of a number smaller than that of bits required of the data for the request by means of packetizing whereas the rest of the claims do not include the said substantial parts as indispensable claim elements. Nor do they have an object common in with that of said Claims 1, 2 and 15-18.

Thus, this application does not conform with the provision of Article 37 of the Patent Law and the claims other than Claims 1-3 and 15-18 were not examined except in light of the provision of said Article 37.

Claim 3 was examined because it required no excessive effort.

References cited:

1. Patent Application Laid-Open No. Sho 58-192154
2. Patent Application Laid-Open No. Sho 63-34795
3. Patent Application Laid-Open No. Sho 61-107453
4. Patent Application Laid-Open No. Sho 63-91766
5. Patent Application Laid-Open No. Sho 62-16289

[6. Utility Model Application No. Sho 60-42584
(Utility Model Application Laid-Open No. Sho 61-160556)]

* * * * *

If new ground for rejection thereon is found, further notice will be given.